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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/845,329	05/01/2001	Martin Martin San Juan	550-228	2248

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EXAMINER	
CHO, HONG SOL	

ART UNIT	PAPER NUMBER
2662	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/845,329	SAN JUAN, MARTIN MARTIN	
	Examiner	Art Unit	
	Hong Cho	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 11* is/are rejected.

7)☒ Claim(s) *3-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05-01-2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05012001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(b) that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, and 11 are rejected under 35 U.S.C. 102(b) as being unpatentable over Rabe et al (U.S 5717873), hereinafter referred to as Rabe.

Re claims 1 and 11, Rabe discloses transferring data in a computer system utilizing multiple buses and a bridge circuit of a system input/output (SIO) circuit for controlling and accomplishing the transfer of data among the CPU, main memory, and the PCI bus (*a slave interface mechanism associated with each slave logic unit in said subset and comprising switching logic arranged to connect either the first bus or the second bus to the corresponding salve logic unit to enable either the first transfer request or the second transfer request to be routed to that slave logic unit*, column 4, lines 31-33). Rabe discloses a bridge circuit for joining a bus master (*a first master logic unit*) to a PCI bus (*a first bus*) adapted to carry information to various components of the system (*a first bus for coupling a first master logic unit with a plurality of slave logic units to enable the first master logic unit to issue a first transfer request to any of said slave logic units*,

column 4, lines 9-13). A bus master is a component of originating and controlling the transfer of data such as a direct memory access (DMA) unit (column 1, line 67 to column 2, line 2). Rabe discloses a bridge circuit granting a bus master (*a second master logic unit*) to access the secondary bus (*a second bus*) (*a second bus for coupling a second master logic unit with a subset of said plurality of slave logic units to enable the second master logic unit to issue a second transfer request to any of the slave logic units in said subset*, column 3, lines 2-5*)*.

Re claim 2, Rabe discloses an arbitration arrangement to overcome the deadlock condition in which a PCI bus master wants to write to a device on the ISA bus while an ISA bus master has gained access to the ISA bus to read from main memory by letting an ISA bus master complete the read operation first (*a slave interface mechanism comprising an arbitration control unit for applying predetermined criteria to control the routing of the first and second transfer requests to the corresponding slave logic unit in the event that the slave logic unit is already processing one of the transfer requests when the other transfer request is issued to the slave logic unit*, column 7, line 40 to column 9, line 20).

Allowable Subject Matter

3. Claims 3-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

4. Claims 3-10 are allowable over the prior art of record since the cited references taken individually or in combination fails to particularly disclose requesting burst data transfer comprising a non-sequential transfer request followed by a number of sequential transfers, and the predetermined criteria applied by the arbitration control unit is such that upon issuance of a non-sequential transfer request from one of said master logic units, the slave interface mechanism will defer routing that non-sequential transfer request to the slave logic unit until any burst transfer request already being handled by that slave logic unit has been completed, as specified in an independent claim 1. It is noted that the closest prior art of record, Rabe shows a method of overcoming the deadlock condition in which a PCI bus master wants to write to a device on the ISA bus while an ISA bus master has gained access to the ISA bus to read from main memory by letting an ISA bus master complete the read operation first. However, Rabe fails to suggest handling a non-sequential transfer request followed by a number of sequential transfers as required by the claimed invention.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US Patent (5544332) to Chen discloses method for preventing deadlock in a multi-bus computer system

- US Patent (5943483) to Solomon discloses controlling access to a bus in a data processing system

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Cho whose telephone number is 571-272-3087. The examiner can normally be reached on Mon-Fri during 7 am to 4 pm.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-3088.
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hong Cho
Patent Examiner
12-01-2004

RICKY NGO
PRIMARY EXAMINER